

REMARKS

A supplemental declaration under 37 C.F.R. § 167(a)(2) is attached hereto to satisfy the objection to the declaration.

Claims 1 and 6 have been amended to include in the list of incremental changes all polygons added and all polygons deleted from the integrated circuit design by the engineering change order. Support for the amendment may be found in the specification on page 11, line 26 to page 12, line 2.

Claims 1-10 are pending in the application.

By way of this response, Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that the examiner telephone Peter Scott at (719)533-7969 so that such issues may be resolved as expeditiously as possible.

Response to the rejection under 35 U.S.C. § 103

Claims 1 and 6 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Morgan, U.S. Patent 6,530,073 (*Morgan*) in view of Falbo, U.S. Patent Publication 2003/0163791 (*Falbo*). Applicant respectfully traverses the rejection as follows.

As explained in the specification on page 11, line 26 to page 12, line 2, the claimed list of incremental changes recited in Claims 1 and 6 includes all polygons added and all polygons deleted from the integrated circuit design by the engineering change order. In contrast to Claims 1 and 6, *Morgan* does not define incremental changes to the integrated

circuit design in terms of adding and deleting polygons. Further, the incremental changes cited by the rejection in *Morgan*, column 11, lines 35-40, are not described as being included in a list of incremental changes. Consequently, the incremental changes cited by the rejection in *Morgan* are not equivalent to the claimed list of incremental changes that includes all polygons added to the integrated circuit design and all polygons deleted from the integrated circuit design by the engineering change order. Because *Morgan* does not teach or suggest the claimed list of incremental changes that includes all polygons added to the integrated circuit design and all polygons deleted from the integrated circuit design by the engineering change order, *Morgan* does not teach or suggest step (e) as alleged by the rejection. Because *Morgan* does not teach or suggest step (e), the modification of *Morgan* proposed by the rejection fails to arrive at the claimed invention. Because the modification of *Morgan* proposed by the rejection fails to arrive at the claimed invention, Claims 1 and 6 are not obvious under 35 U.S.C. § 103(a).

Claims 2-5 and 7-10 stand rejected under 35 U.S.C. § 103(a) as unpatentable over *Morgan* in view of *Falbo*, and further in view of Sung, U.S. Patent Publication 2005/0216872 (*Sung*). Applicant respectfully traverses the rejection as follows.

Regarding Claims 2 and 7, the rejection alleges that *Sung* teaches translating the claimed marked integrated circuit design database to a file in generic data stream format on page 4, paragraph [0044]. In contrast to Claims 2 and 7, *Sung* teaches generating a GDS file from a physical view that represents the cumulative reticle layers that form the semiconductor features on the integrated circuit. *Sung* does not teach or suggest translating the claimed marked integrated

circuit design database. Because *Sung* does not translate the claimed marked integrated circuit design database to generate the GDS file, there is no basis for assuming that the resulting GDS file in *Sung* would be equivalent to the claimed file in generic data stream format. Because there is no basis for assuming that the resulting GDS file in *Sung* would be equivalent to the claimed file in generic data stream format, *Sung* does not teach or suggest translating the claimed marked integrated circuit design database to the claimed file in generic data stream format as alleged by the rejection. Because *Sung* does not teach or suggest translating the claimed marked integrated circuit design database to a file in generic data stream format as alleged by the rejection, the modification of *Morgan* proposed by the rejection fails to arrive at the claimed invention. Because the modification of *Morgan* proposed by the rejection fails to arrive at the claimed invention, Claims 2 and 7 are not obvious under 35 U.S.C. § 103(a).

Regarding Claims 3 and 8, the rejection alleges that *Morgan* teaches the claimed step of applying a special rule deck to validate the marked integrated circuit design database wherein the special rule deck includes only design checks and rules applicable to the polygons in the generic data stream file that were changed from the current state in column 1, lines 35-40 and column 9, lines 32-51. In contrast to Claims 3 and 8, *Morgan* does not teach or suggest either the claimed polygons or the claimed special rule deck that includes only design checks and rules applicable to the polygons in the generic data stream file that were changed from the current state as alleged by the rejection. Because *Morgan* does not teach or suggest either the claimed polygons or the claimed special rule deck that includes only design checks and rules

applicable to the polygons in the generic data stream file that were changed from the current state as alleged by the rejection, the modification of *Morgan* proposed by the rejection fails to arrive at the claimed invention. Because the modification of *Morgan* proposed by the rejection fails to arrive at the claimed invention, Claims 3 and 8 are not obvious under 35 U.S.C. § 103(a).

Regarding Claims 4 and 9, the rejection alleges that *Morgan* teaches the claimed step of identifying a design rule violation in the polygons in the generic data stream file that were changed from the current state in column 1, lines 40-50; FIG. 1B; and column 10, lines 45-50. In contrast to Claims 4 and 9, *Morgan* does not teach or suggest the claimed polygons or the claimed design rule violation in the polygons. Because *Morgan* does not teach or suggest either the claimed polygons or the claimed design rule violation in the polygons as alleged by the rejection, the modification of *Morgan* proposed by the rejection fails to arrive at the claimed invention. Because the modification of *Morgan* proposed by the rejection fails to arrive at the claimed invention, Claims 4 and 9 are not obvious under 35 U.S.C. § 103(a).

Regarding Claims 5 and 10, the rejection alleges that *Morgan* teaches the claimed step of modifying the marked integrated circuit design database to correct the design rule violation in FIG. 1A (90). As explained above, *Morgan* does not teach or suggest the claimed polygons or the claimed design rule violation in the polygons. Because *Morgan* does not teach or suggest the claimed design rule violation in the polygons, the modification of *Morgan* proposed by the rejection fails to arrive at the claimed invention. Because the modification of *Morgan* proposed by the rejection fails to arrive at the claimed invention, Claims 5 and 10 are not

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obvious under 35 U.S.C. § 103(a).

Applicant respectfully requests examination and
favorable reconsideration of Claims 1-10.

No additional fee is believed due for this
amendment.

Respectfully submitted,
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